In claim 10, line 1, change "9" to -- 8 -- .

REMARKS

This application has been reviewed in light of the Office action dated October 16, 1998. Claims 1-5, 7-8 and 10 are pending in the application. Claim 9 has been canceled without prejudice. The Examiner's objection is therefore moot. Claims 6 and 11 have also been canceled without prejudice. Claim 1 has been amended to include the subject matter of claim 6, and Claim 8 has been amended to include the subject matter of claims 9 and 11. No new matter has been added. Claims 7 and 10 has been amended to change their dependency. The examiner's reconsideration of the rejection in view of the amendments and the following remarks is respectfully requested.

By the office action, claims 1, 8, 9 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fukuda (Japanese Patent No. 57-159038 hereinafter Fukuda) in view of Wolf. The Examiner stated that Fukuda includes the claimed trench isolation structure in FIGS. 4a-4e of Fukuda. The Examiner takes Official Notice that a dielectric layer (TEOS) is the equivalent of polysilicon for filling trenches.

Fukuda is directed to a method for forming V-shaped isolation regions. It appears that Fukuda fills a trench with polysilicon material and prevents the formation of an N-channel in the polysilicon (see Constitution, last two lines) by forming a nitride isolation layer 12'. The nitride layer 12' remaining in the trench provides extra isolation between the conducting polysilicon 5 and a P type semiconductor region in a semiconductor substrate 10 (see Purpose of Fukuda). As is known in the art, a P-well is generally located a greater depth in a substrate. It is believed by the Applicant that the title of Fukuda, "Forming Method for V-shaped Isolation Region" refers only to the nitride piece 12' left remaining only in the bottom of the trench. It appears that this nitride layer 12' provides additional isolation between the P type region below and the polysilicon above to prevent interaction therebetween. As polysilicon is a conductor, as known

in the art, as described in VLSI Technology, Second Edition, by S.M. Sze on page 233, a copy of which is attached herewith, it is submitted that one skilled in the art would not use a conductive material to form an electrical isolation region. The polysilicon of Fukuda may be a metal line or other conductive component. It appears that Fukuda does not suggest an isolation region disposed between transistor devices as in the Applicants' invention.

Wolf is cited by the Examiner to show depths of isolation devices. These devices are known in the art and their depths are also known. However, the art cited does not teach or suggest a nitride liner disposed below a transistor channel depth. Wolf does not cure the deficiencies of Fukuda in this respect nor does Wolf cure the deficiencies with respect to filling the trench with polysilicon to provide isolation.

The Applicants' claimed invention, as amended, includes, *inter alia*, an oxide fill disposed above said nitride liner such that said oxide fill extends above the uppermost of said nitride liner to substantially a top surface of said substrate, such that substantially no polysilicon material is disposed within the trench and said nitride liner is disposed below a transistor channel depth of a transistor. Fukuda teaches away from the Applicants' invention. Fukuda uses a known conductor to fill the trench. The Applicants fill the trench with a dielectric to avoid polysilicon from getting into the trench. Fukuda and/or Wolf do not disclose or suggest a nitride liner disposed below a transistor channel depth. In fact, it is believed that the Fukuda patent is a completely different invention which would not lead one skilled in the art to the Applicants' invention, and Wolf does not cure this deficiency.

The Examiner takes Official Notice that polysilicon and TEOS are equivalents for filling a trench. The Applicant agree that both materials are used in the art. However, the Applicants respectfully disagree that the materials are equivalents. Trenches used for conducting, for example, deep trench capacitors are filled with polysilicon to provide a conductive storage node. Isolators are filled with an isolating material, as taught by the Wolf reference, and not filled with a conducting material as the Examiner suggests Fukuda teaches. The Applicants' invention provides a solution to charge trapping of isolation regions adjacent to active devices. The

structure claimed by the Applicant is not disclosed or suggested by the cited references, either alone or in combination. In fact, it is believed that no motivation exists to combine the cited references to arrive at the present invention.

The afore-mentioned fundamental differences between Fukuda and Wolf and the presently claimed invention provide sufficient basis to reverse this rejection. The cited references either alone or in combination do not teach or suggest a shallow trench isolator which includes, *inter alia*, an oxide fill disposed above said nitride liner such that said oxide fill extends above the uppermost of said nitride liner to substantially a top surface of said substrate, such that substantially no polysilicon material is disposed within the trench and said nitride liner is disposed below a transistor channel depth of a transistor. Accordingly, withdrawal of the rejection of claims 1 and 8 is respectfully requested for at least the reasons stated. The remaining dependent claims 2-5, 7 and 10 are also believed allowable for at least the reasons stated and based on their dependencies.

In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

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CHAPTER 6

DIELECTRIC AND POLYSILICON FILM DEPOSITION

A. C. ADAMS

6.1 INTRODUCTION

Deposited films are widely used in the fabrication of modern VLSI circuits. These films provide conducting regions within the device, electrical insulation between metals, and protection from the environment. Deposited films must meet many requirements. The film thickness must be uniform and reproducible over each device and over all the wafers processed at one time. The structure and composition of the film must be controlled and reproducible. Finally, the method for depositing the film must be safe, reproducible, easily automated, and inexpensive.

The most widely used materials for film deposition are polycrystalline silicon, silicon dioxide, stoichiometric silicon nitride, and plasma-deposited silicon nitride. The most common deposition methods are atmospheric-pressure chemical vapor deposition (APCVD), low-pressure chemical vapor deposition (LPCVD), and plasma-enhanced chemical vapor deposition (PECVD or plasma deposition). Several reviews of these materials and their preparation are available.[1–3]

Polycrystalline silicon, usually referred to as polysilicon, is prepared by pyrolyzing silane at 575 to 650°C. Polysilicon is used as the gate electrode material in MOS devices, as a conducting material for multilevel metallization, and as a contact material for devices with shallow junctions. Polysilicon is usually deposited without dopants. The doping elements—arsenic, phosphorus, or boron—reduce the resistivity of the polysilicon and are added later by diffusion